## **LAB 5**

## OBJECTIVE: To design and simulate a **Half Adder Circuit** using VHDL, and verify its functionality using a testbench.

## TOOLS USED:

* VHDL (VHSIC Hardware Description Language)
* <https://www.edaplayground.com/> (for simulation)

**THEORY:**

A Half Adder is a basic combinational circuit that adds two single-bit binary numbers. It produces two outputs:

* Sum (S): XOR of inputs A and B
* Carry (C): AND of inputs A and B

## VHDL CODE

**DESIGN**

library ieee;

use ieee.std\_logic\_1164.all;

entity ha is

port( a: in std\_ulogic;

b: in std\_ulogic;

c: out std\_ulogic;

s: out std\_ulogic);

end ha;

architecture behave of ha is

begin

s <= a xor b;

c <= a and b;

end behave;

**TESTBENCH**

library ieee;

use ieee.std\_logic\_1164.all;

entity ha\_testbench is

end ha\_testbench;

architecture test of ha\_testbench is

component ha

port(a: in std\_ulogic;

b: in std\_ulogic;

c: out std\_ulogic;

s: out std\_ulogic);

end component;

signal ain, bin, carry, sum : std\_logic;

begin

half\_adder: ha port map (a => ain, b => bin, c => carry, s => sum);

process begin

ain <= '0'; bin <= '0'; wait for 1 ns;

ain <= '0'; bin <= '1'; wait for 1 ns;

ain <= '1'; bin <= '0'; wait for 1 ns;

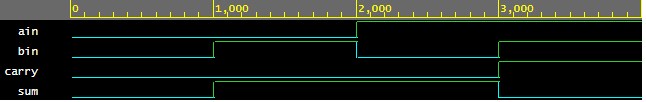
ain <= '1'; bin <= '1'; wait for 1 ns;

assert false report "Reached end of test";wait;

end process;

end test;

Output:



CONCLUSION:

The Half Adder was successfully implemented and simulated in VHDL. The outputs of the simulation matched the expected values based on the truth table of a half adder. The testbench applied all input combinations and validated the behavior effectively.